美浦森半导体
M s e m i t e k

RoHS
LEAD FREE

SLN30L03A
N And P-Channel Enhancement Mode MOSFET

General Description

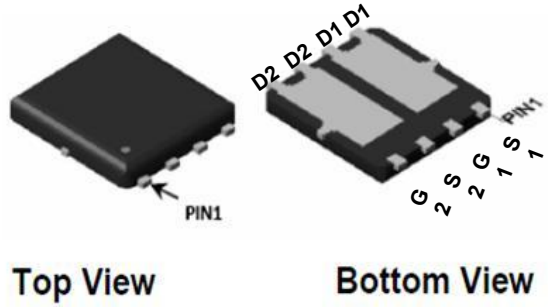
This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

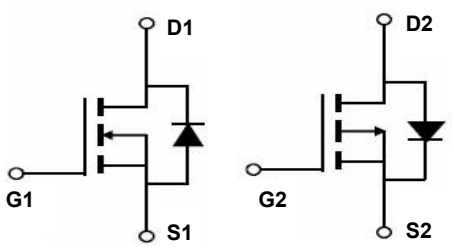
☑ PWM Application
☑ Load Switch
☑ Power Management

Features

- N-Channel: 30V 20A
  $R_{DS(on)Typ}$= 10.5mΩ@V_{GS} = 10 V
  $R_{DS(on))Typ}$= 15.5mΩ@V_{GS} = 4.5V
- P-Channel: -30V- 20A
  $R_{DS(on))Typ}$= 26mΩ@V_{GS} = -10 V
  $R_{DS(on))Typ}$=36mΩ@V_{GS} = -4.5V
- Very Low On-resistance RDS(ON)
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



DFN3*3 -Double base



N-Channel P-Channel

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
I_D	Drain Current - Continuous (T_C = 25℃)	20	-20	A
	- Continuous (T_C = 100℃)	14	-13	A
I_{DM}	Drain Current - Pulsed (Note 1)	120	-60	A
V_{GSS}	Gate-Source Voltage	±20	±20	V
P_D	Power Dissipation (T_C = 25℃)	2.7	5.4	W
$R_{\theta Jc}$	Thermal Resistance, Junction to Case	46	2.3	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLN30L03A	SLN30L03A	DFN3*3 Double base	Tape & Reel	5000	50000

N-Channel Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 30 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 24 V, T_C = 125℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	1.0	-	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8A	--	10.5	13	mΩ
		V_{GS} = 4.5 V, I_D =4A	-	15.5	20	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 30A	--	15	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	--	1116	-	pF
C_{oss}	Output Capacitance		--	187	-	pF
C_{rss}	Reverse Transfer Capacitance		--	152	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= 10 V, V_{DS}=15 V, R_L = 2.5 Ω ;ID=15 A	--	15	--	ns
t_r	Turn-On Rise Time		--	19	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	--	ns
t_f	Turn-Off Fall Time		--	21	--	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D =15A, V_{GS} = 10 V	--	18.3	--	nC
Q_{gs}	Gate-Source Charge		--	3.9	--	nC
Q_{gd}	Gate-Drain Charge		--	5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	30	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	120	A

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

P-Channel Electrical Characteristics

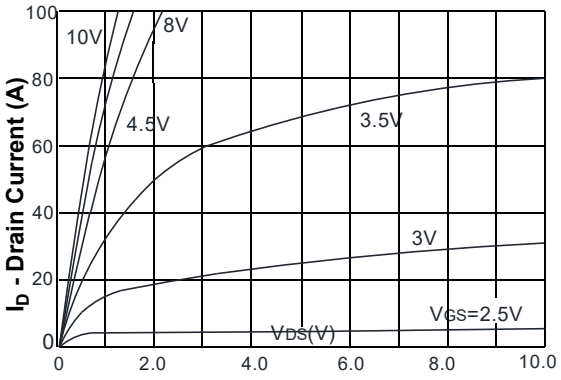
T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -30 V, V_{GS} = 0 V	--	--	-1	uA
		V_{DS} = -24 V, T_C = 125℃	--	--	-10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D =- 250 uA	-1.0	-	-2.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -15A	--	26	34	mΩ
		V_{GS} = -4.5 V, I_D = -10A	-	36	46	
g_{FS}	Forward Transconductance	V_{DS} = -5V, I_D = -20A	--	18	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	--	2800	-	pF
C_{oss}	Output Capacitance		--	346	-	pF
C_{rss}	Reverse Transfer Capacitance		--	319	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= -10 V, V_{DS}= -15 V, R_L = 2.3 Ω ,ID= -20 A	--	14	--	ns
t_r	Turn-On Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	--	ns
t_f	Turn-Off Fall Time		--	65	--	ns
Q_g	Total Gate Charge	V_{DS} =-15 V, I_D =-20A, V_{GS} =-10 V	--	28	--	nC
Q_{gs}	Gate-Source Charge		--	5.3	--	nC
Q_{gd}	Gate-Drain Charge		--	7.6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-10	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-40	A

Notes:

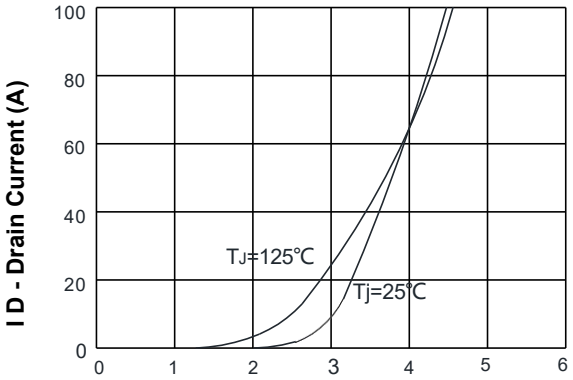
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

N- Channel Typical Characteristics



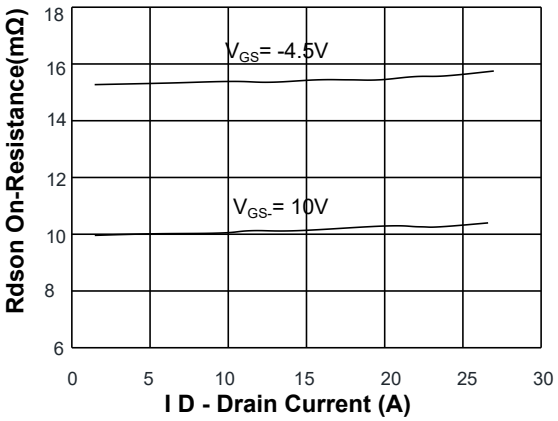
Vds Drain-Source Voltage (V)

Figure 1. On-Region Characteristics



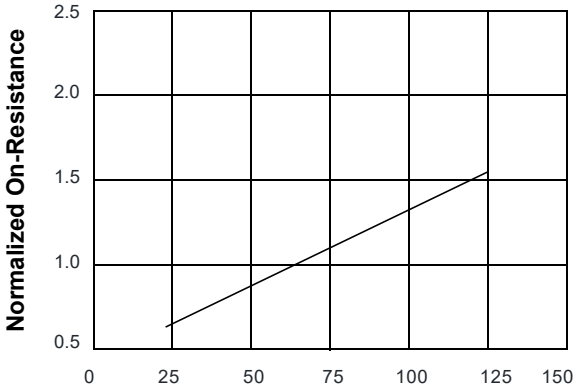
Vgs Gate-Source Voltage (V)

Figure 2. Transfer Characteristics



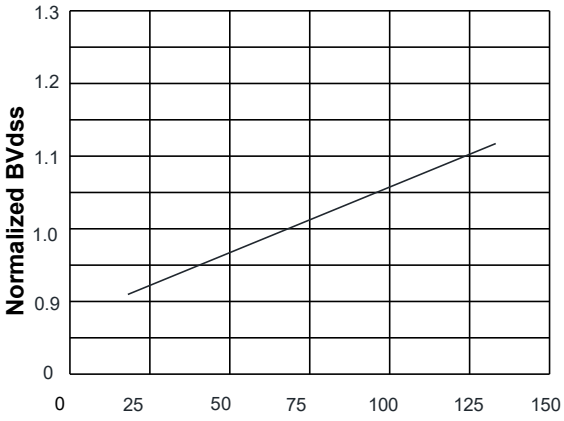
I D - Drain Current (A)

Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage



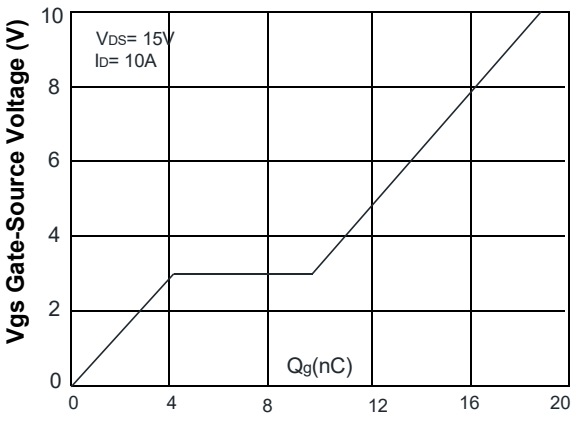
T J -Junction Temperature(℃)

Figure 4. On-Resistance Variation vs Temperature



Vgs Gate-Source Voltage (V)

Figure 5. On-Resistance Variation vs Temperature



Qg Gate Charge (nC)

Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

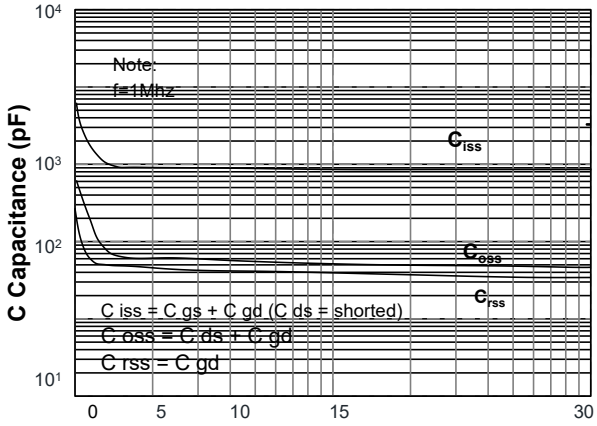


Figure 7. Capacitance vs Vds

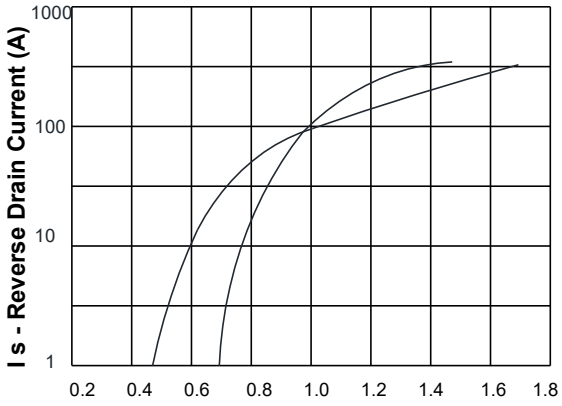


Figure 8. Reverse Drain Current vs Temperature

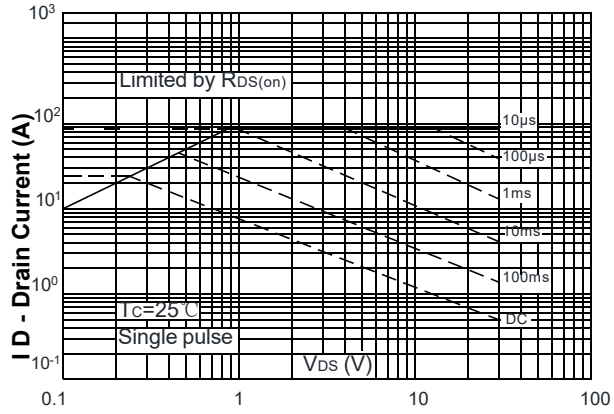


Figure 9. Maximum Safe Operating Area

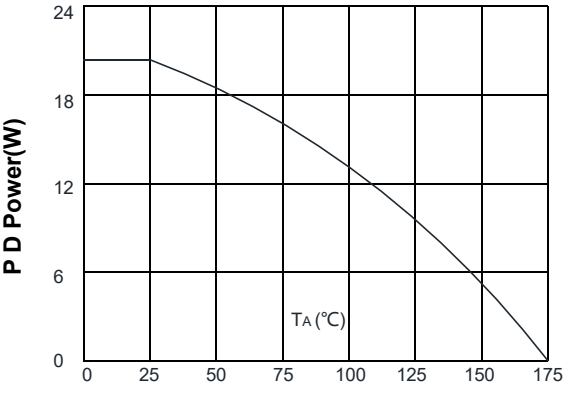


Figure 10. Maximum Power Dissipation vs Temperature

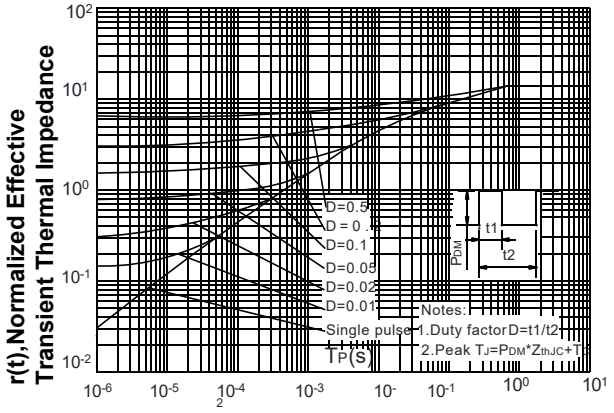
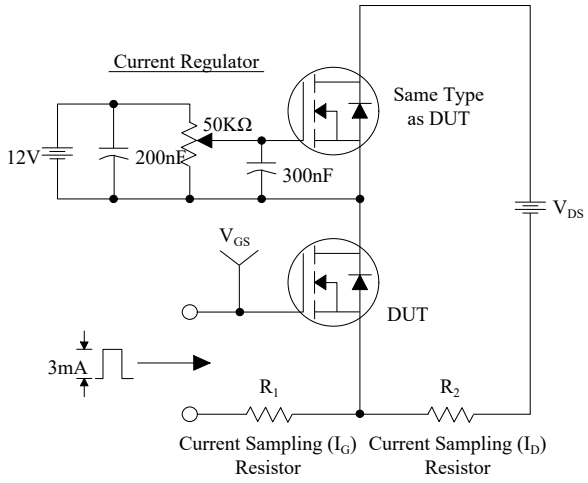
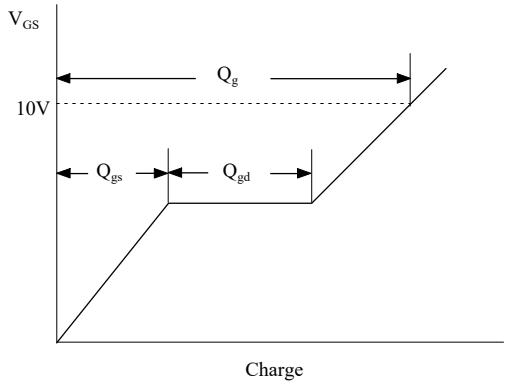


Figure 11. Transient Thermal Response Curve

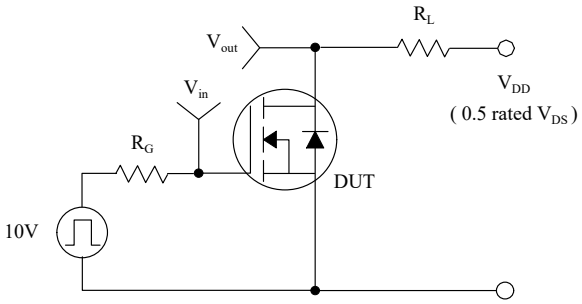
N- Channel

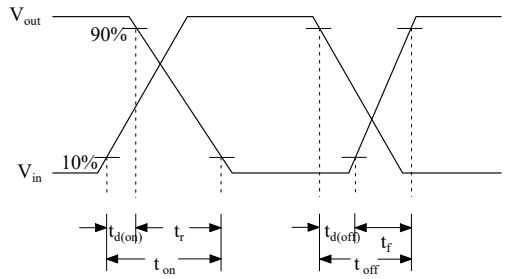
Gate Charge Test Circuit & Waveform



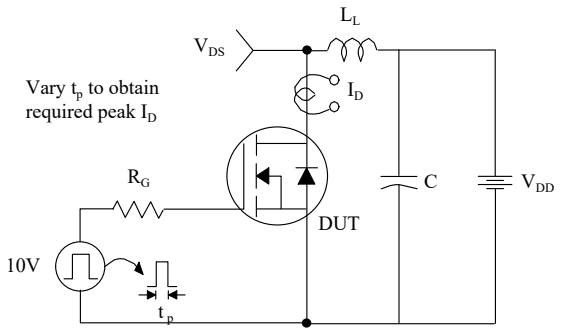


Resistive Switching Test Circuit & Waveforms

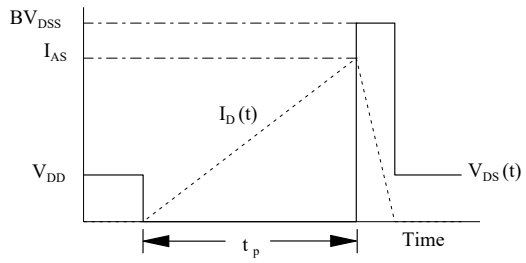




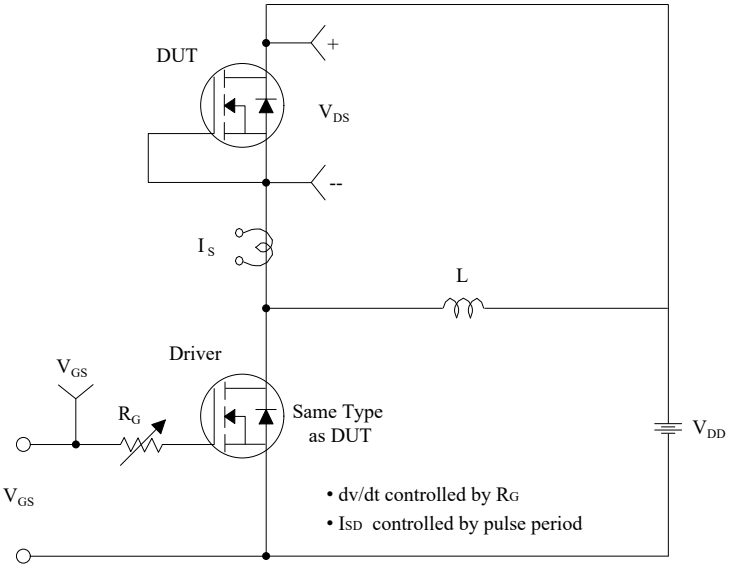
Unclamped Inductive Switching Test Circuit & Waveforms

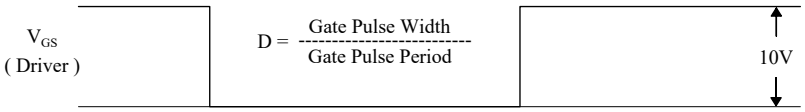


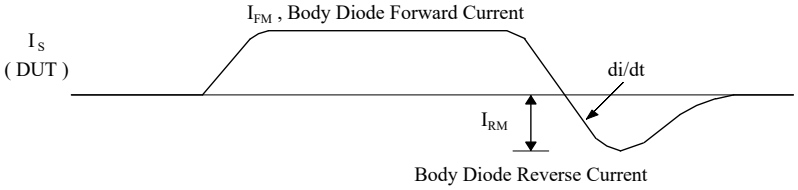
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

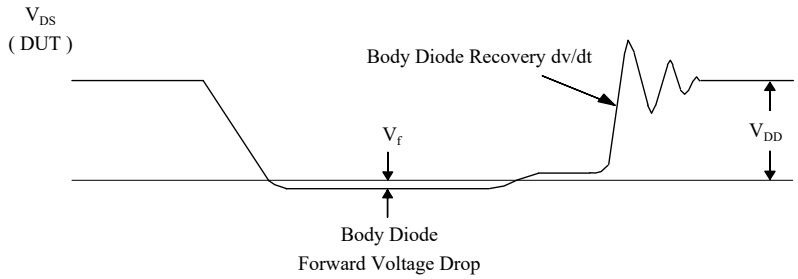


N- Channel Peak Diode Recovery dv/dt Test Circuit & Waveforms









P- Channel Typical Characteristics

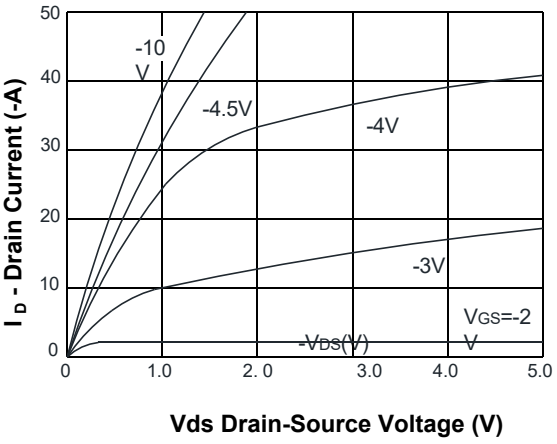


Figure 1. On-Region Characteristics

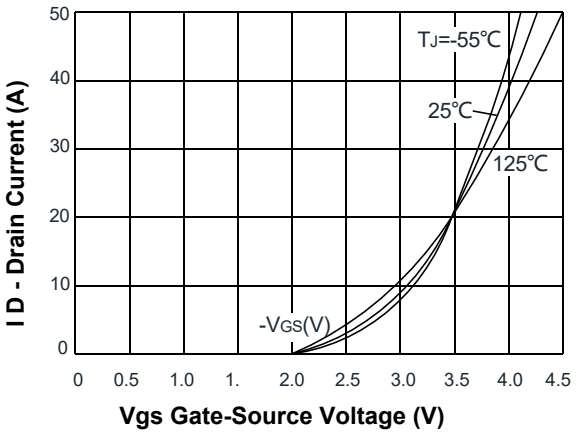


Figure 2. Transfer Characteristics

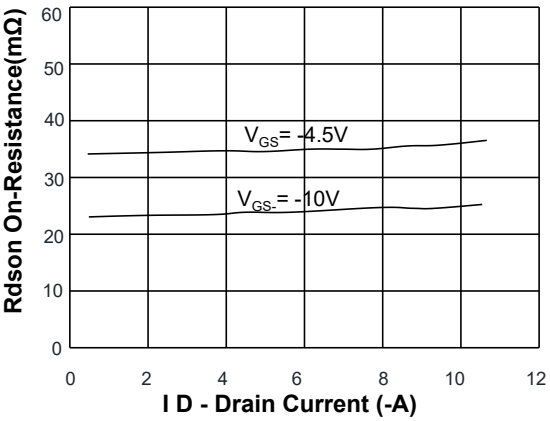


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

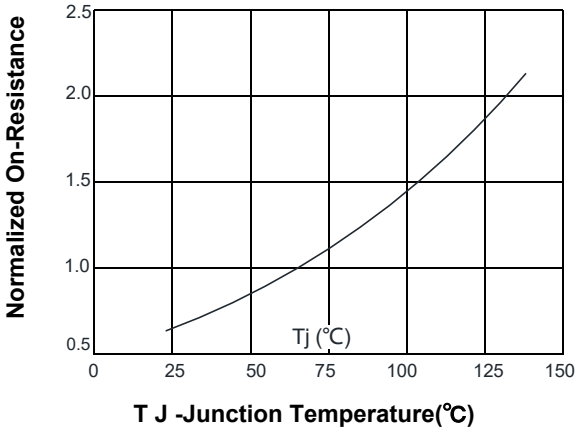


Figure 4. On-Resistance Variation vs Temperature

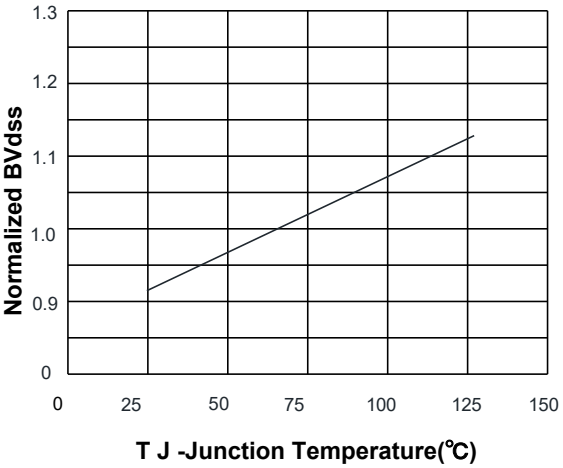


Fig ure 5. BV DSS vs Junction Temperature

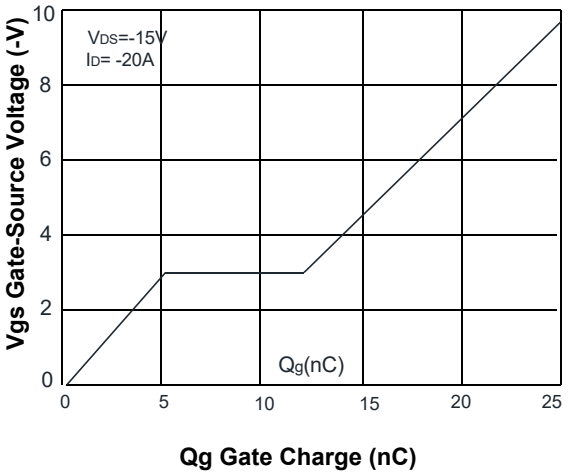


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

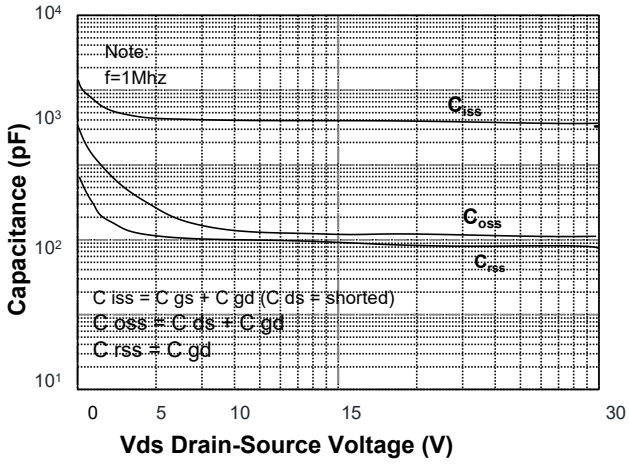


Figure 7. Capacitance vs Vds

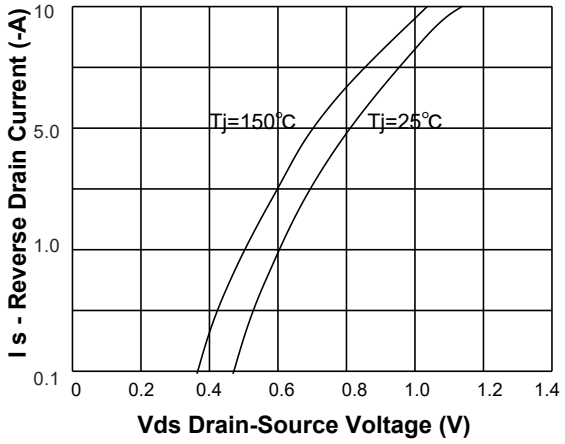


Figure 8. Reverse Drain Current vs Temperature

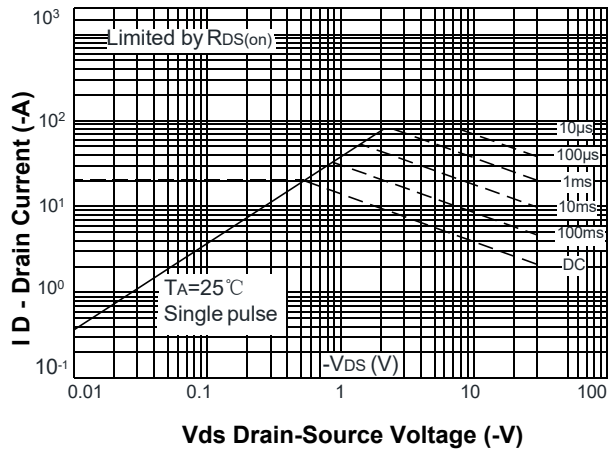


Figure 9. Maximum Safe Operating Area

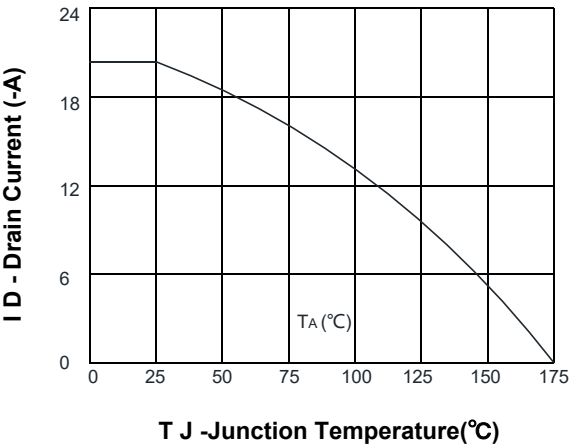


Figure 10. Maximum Drain Current vs Temperature

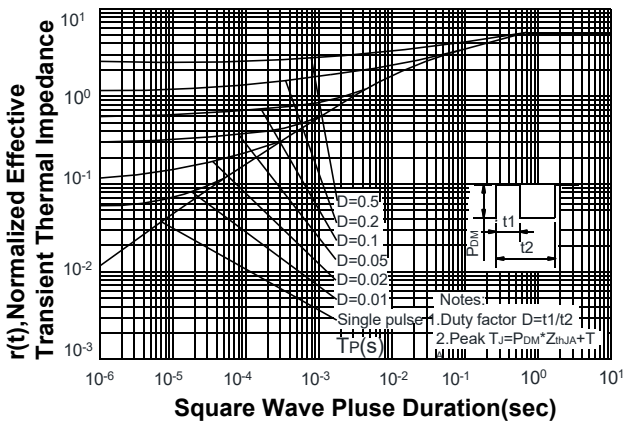
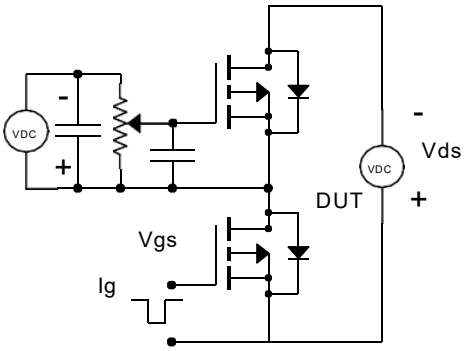
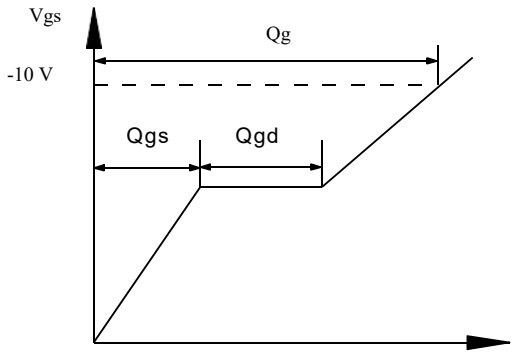


Figure 11. Transient Thermal Response Curve

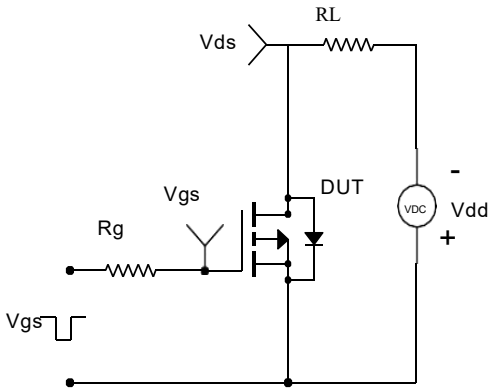
P- Channel

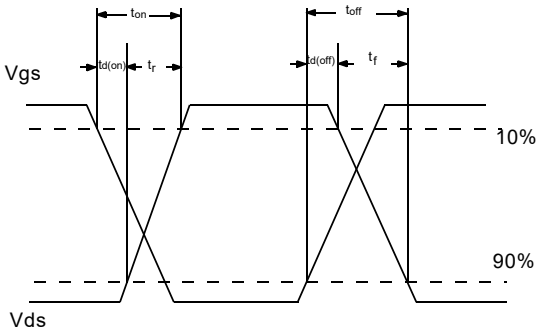
Gate Charge Test Circuit & Waveform



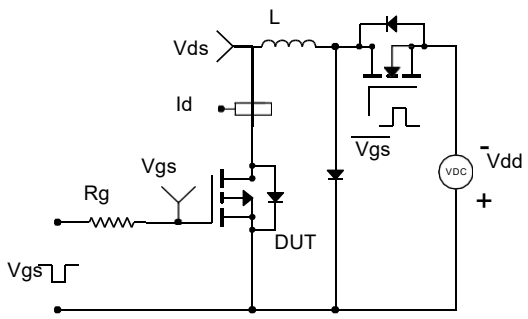


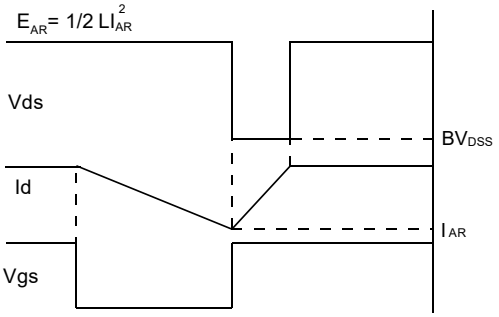
Resistive Switching Test Circuit & Waveforms





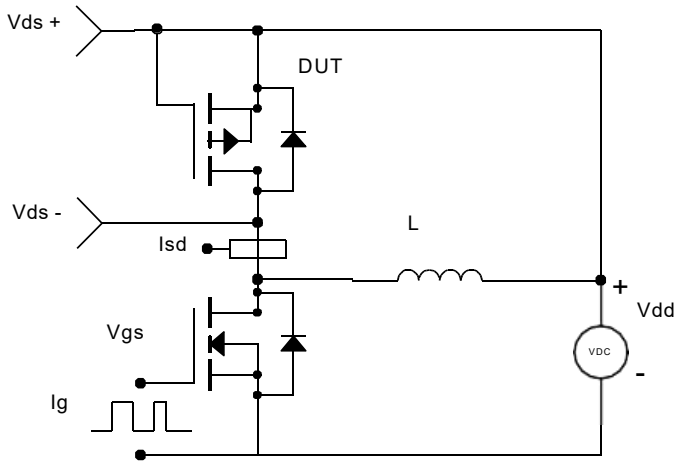
Unclamped Inductive Switching Test Circuit & Waveforms



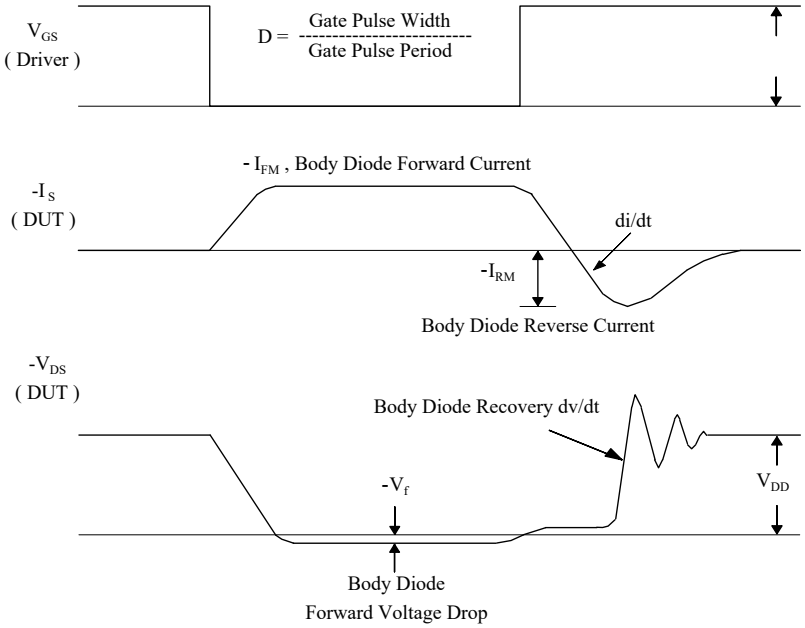


P- Channel

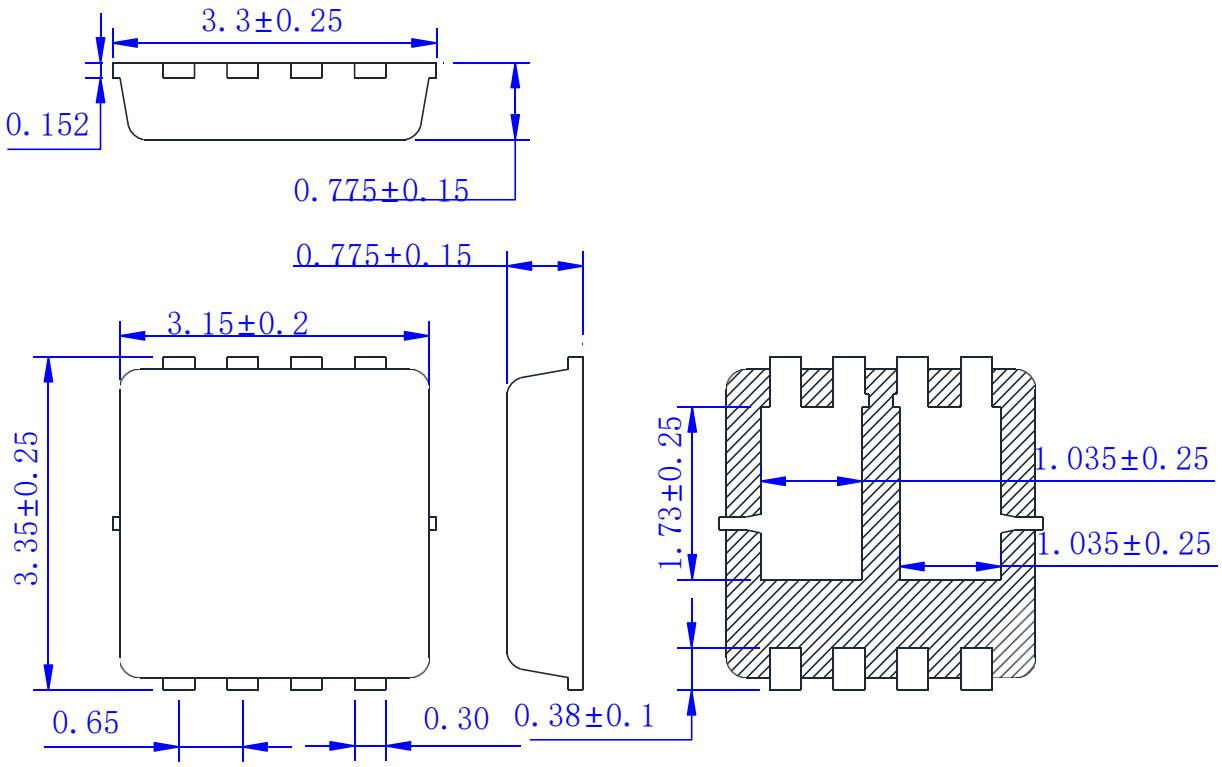
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



DFN 3*3 Double Base OUTLINE



NOTE:
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

NAME	DFN3*3-Double OUTLINE	UNIT	mm	DESIGNED	Shawn Chen	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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