



SLP25N10T 100V N -Channel MOSFET

General Description

This Power MOSFET is produced using Msemitek's advanced TRENCH technology.

This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

☑PWM Application

☑Power Management

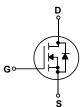
Features

- N-Channel:100V 25A

$$R_{DS(on)Typ}$$
= 40m $\Omega@V_{GS}$ = 10 V $R_{DS(on)Typ}$ = 45m $\Omega@V_{GS}$ =4.5 V

- Very Low On-resistance R_{DS(ON)}
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLP25N10T	Units
V_{DSS}	Drain-Source Voltage	100	V
	Drain Current - Continuous (T _C = 25°C)	25	Α
I_D	- Continuous (T _C = 100°C)	100	Α
I_{DM}	Drain Current - Pulsed (Note 1)	100	Α
V_{GSS}	Gate-Source Voltage	±20	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	39	mJ
PD	Power Dissipation (T _C = 25°C)	54	W
R _{0JC}	Thermal Resistance, Junction to Case	2.78	°C/W
R _{0JA}	Thermal Resistance, Junction to ambient	55	°C/W
T_J , T_{STG}	Operating and Storage Temperature Range	-55 to +175	တ
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	ဇ

^{*} Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLP25N10T	SLP25N10T	T0-220C	Tube	1000	5000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100 V, V _{GS} = 0 V	-	-	1.0	uA
Igssf	Gate-Body Leakage Current, Forward	V _{GS} = 20V, V _{DS} = 0 V	-		100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \text{ uA}$	1.0	1.5	3.0	٧
R _{DS(on)}	Static Drain-Source	V _{GS} = 10 V, I _D = 20A	40	50	mΩ	
	On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{A}$		45	55	mΩ

Dynamic Characteristics

Ciss	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	1	2210	-	pF
Coss	Output Capacitance		1	85.1	-	pF
C _{rss}	Reverse Transfer Capacitance	1.0 1/11/2		70	-	pF

Switching Characteristics

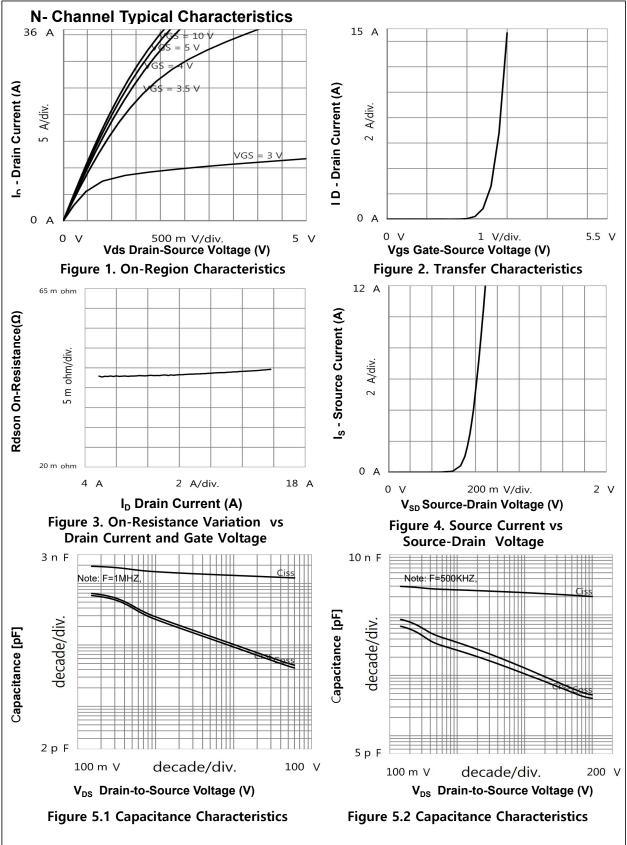
$t_{d(on)}$	Turn-On Delay Time		 10		ns
t _r	Turn-On Rise Time	V_{GS} = 10 V, V_{DS} =30V, R_L = 1.8 Ω , I_D =10A (Note 3)	 19		ns
t _{d(off)}	Turn-Off Delay Time	11C = 1.0 12 ,,1D=10A (Note 5	 42	-	ns
t_f	Turn-Off Fall Time		 26	-	ns
Q_g	Total Gate Charge	V _{DS} = 30 V, I _D =10A,	 41.9	-	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10V$ (Note 3	 9.1	-	nC
Q_{gd}	Gate-Drain Charge		 11.5		nC

Drain-Source Diode Characteristics and Maximum Ratings

Is	Maximum Continuous Drain-Source Diode Forward Current			25	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-		100	Α
VF _{SD}	Drain to Source Diode Forward Voltage, V GS = 0V, I SD = 20A, T J = 25°C	1	-	1.2	V
Trr	Reverse recovery time,I _F =10A D _I /dt=100A/μs		37		ns
Qrr	Reverse recovery charge,I _F =10A D _{IF} /dt=100A/µs		35.5		nC

Notes:

- 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- 2. EAS condition: T J =25°C, V $_{\rm DD}$ =30V, V $_{\rm G}$ =10V, L=0.5mH, I $_{\rm AS}$ =12.5A 3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



10 V

N- Channel Typical Characteristics (Continued) Position of the property of th

35 n C

Figure 6. Gate Charge Characteristics

Qg Gate Charge (nC)

5 n C/div.

0 C

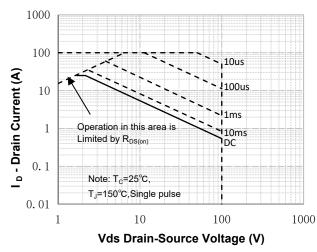
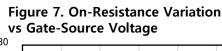


Figure 8. Maximum Safe Operating Area



Vgs Gate-Source Voltage (V)

1 V/div.

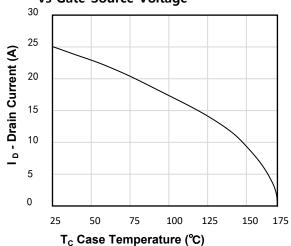
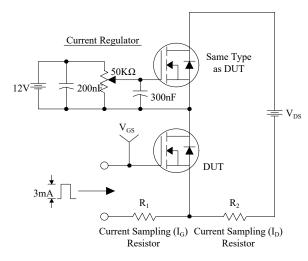
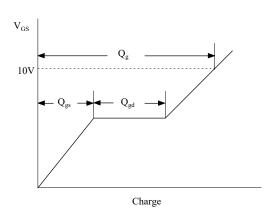


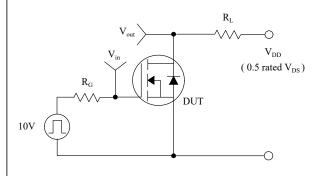
Figure 9. aximum Drain Current vs Case Temperature

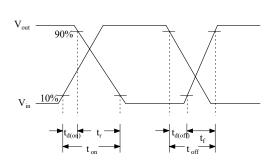
Gate Charge Test Circuit & Waveform



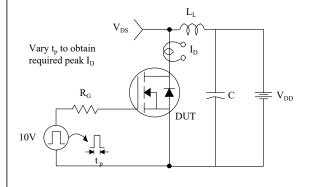


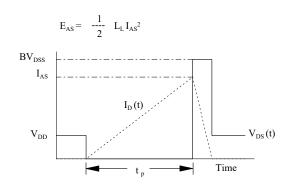
Resistive Switching Test Circuit & Waveforms





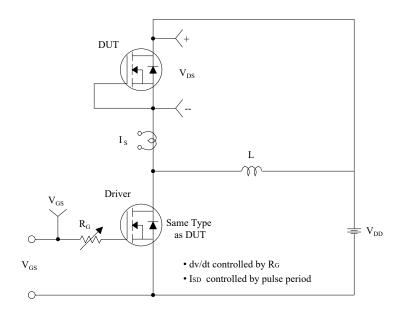
Unclamped Inductive Switching Test Circuit & Waveforms

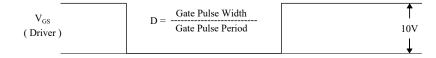


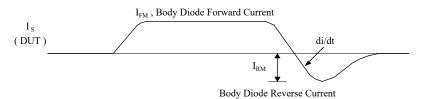


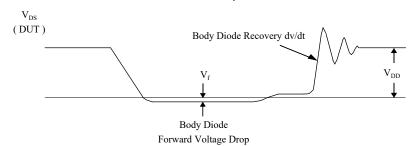
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Peak Diode Recovery dv/dt Test Circuit & Waveforms

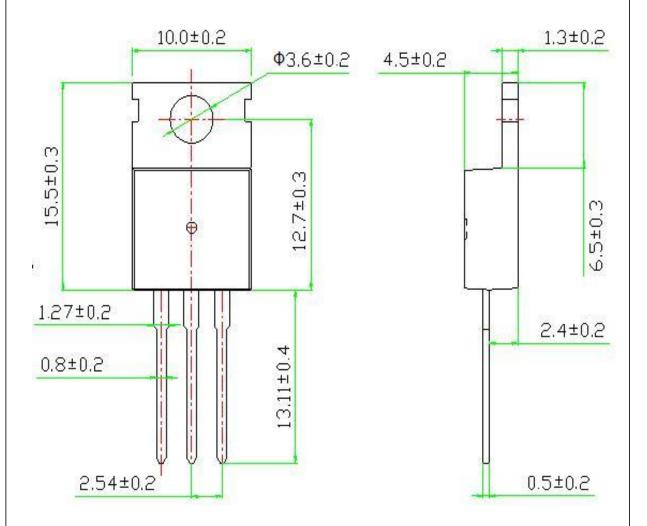








TO-220C OUTLINE



NOTE:

1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8 2.Undeclared tolerance \pm 0.25,Unmarked filletRmax=0.25

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