Maplesemi

LEAD FREE RoHS COMPLIANT

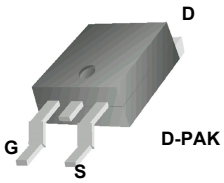
SLD70R900S2 / SLF70R900S2
700V N-Channel Power MOSFET

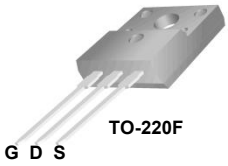
General Description

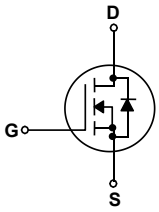
This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology

Features

- 5A, 700V, $R_{DS(on)\ typ.}$ = 0.8Ω@V_{GS} = 10 V
- Extended Safe Operating Area
- Ease of Paralleling
- Fast Switching
- 100% avalanche tested
- 100% Single Pulse avalanche energy Test







Absolute Maximum Ratings

Symbol	Parameter	SLF70R900S2	SLD70R900S2	Units
V_{DSS}	Drain-to-Source Breakdown Voltage	700		V
I_D	Drain Current - Continuous (T_C = 25℃)	5		A
	Drain Current - Continuous (T_C = 100℃)	3.2		A
I_{DM}	Drain Current - Pulsed	18		A
V_{GS}	Gate-Source Voltage	±30		V
Ptot	Power Dissipation (T_C = 25℃)	24	58	W
T_J,	Operating Junction Temperature Range	-55 to +150		℃
EAS	Single Pulsed Avalanche Energy (Note 2)	180		mJ

Electrical Characteristics @ TJ=25℃(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDS	Drain-source Voltage	VGS =0V, ID=250μA	700			V
RDS(on)	Static Drain-to-Source on-Resistance	VGS =10V, ID=20A		0.8	0.9	Ω
VGS(th)	Gated Threshold Voltage	VDS= VGS, ID=250μA	2.0	3.0	4.0	V

IDSS	Zero Gate Voltage Drain Current	VDS=100V, VGS = 0V			1.0	μA
IGSS(F)	Gated Body Leakage Current	VGS = +30V,			100	nA
IGSS(R)	Gated Body Leakage Current	VGS = -30V,			-100	nA
Ciss	Input Capacitance	VGS =0V, VDS=25V, f=1.0MHZ		360		pF
Coss	Output Capacitance			21		pF
Crss	Reverse Transfer Capacitance			1.9		pF
Q_g	Total Gate Charge	V_{DS}=560V I_D=5A V_{GS}=10V		19.2		nC
Q_{gs}	Gate-Source Charge			2.45		nC
Q_{gd}	Gate-Drain Charge			11.7		nC
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=350V,I_D=5A V_{GS}=10V,R_G=24Ω		9.47		nS
t_r	Turn-on Rise Time			26.3		nS
$t_{d(off)}$	Turn-off Delay Time			57.9		nS
t_f	Turn-off Fall Time			25.7		nS

Source-Drain Diode Maximum Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	S-D Current(Body Diode)				5	A
I_{SDM}	Pulsed S-D Current(Body Diode)				18.0	A
VSD	Diode Forward Voltage	VGS =0V, IDS=5A			1.4	V
t_{rr}	Reverse Recovery Time	T_J=25℃,I_F=5A di/dt=100 A/us		305		nS
Q_{rr}	Reverse Recovery Charge			2.3		nC
	*Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%					

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
RθJC	Junction-to-Case		5.21	℃/W
RθJA	Junction-to-Ambient		62.5	℃/W

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 79mH, IAS = 2.0A, VDD =100V, RG = 25Ω, Starting TJ = 25° C
3. ISD 5.0A, di/dt 100A/us, VDD BVDSS, Starting TJ = 25° C
4. Pulse Test : Pulse width 300us, Duty cycle 2%
5. Essentially independent of operating temperature

Typical Characteristics

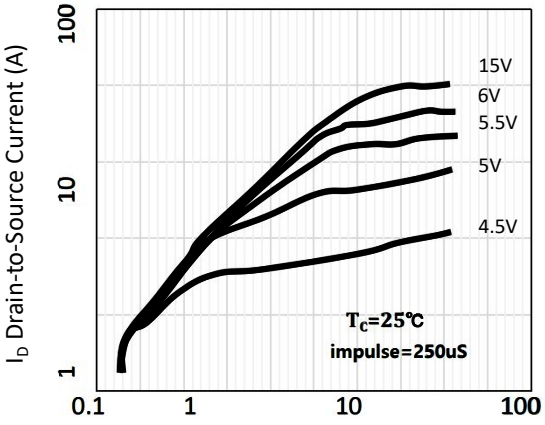


Figure 1. Typical Output Characteristics

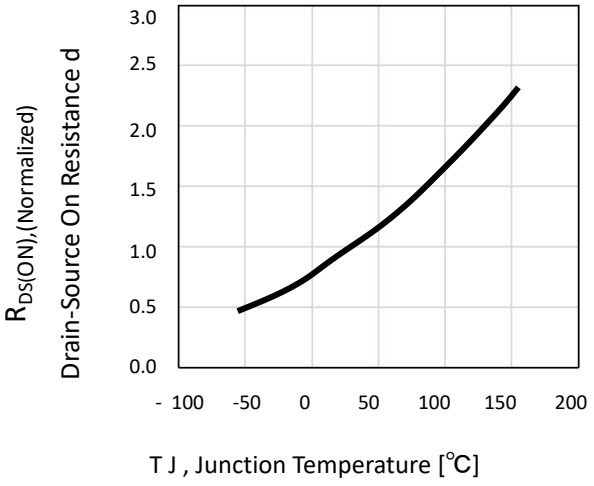


Figure 2. Typical Output Characteristics

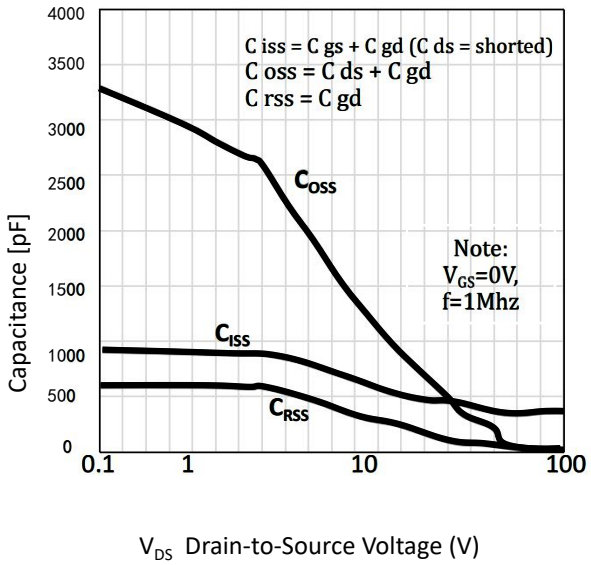


Figure 3. Typical Capacitance Vs Drain-Source Voltage

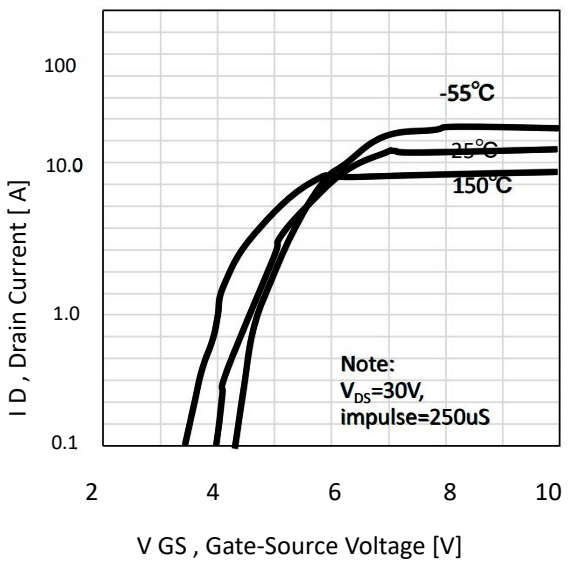


Figure 4. On-Resistance Vs Drain Current

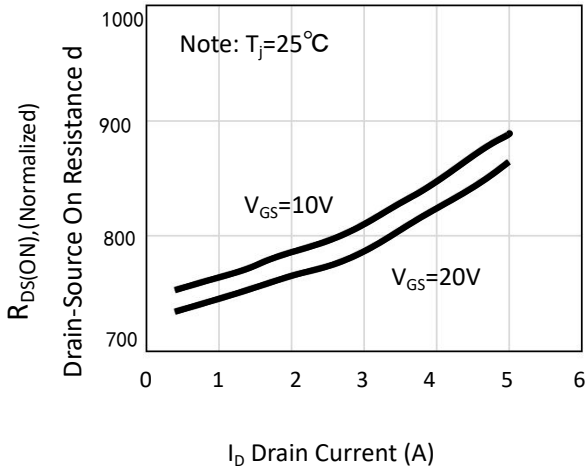


Figure 5. $R_{DS(ON)}$ Vs Drain Current , Gate-Source Voltage

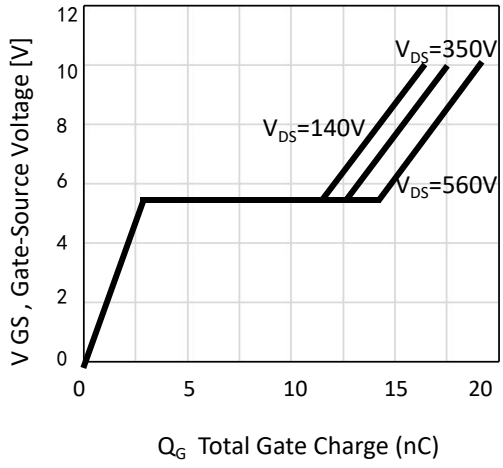


Figure 6. Typical Gate Charge Vs Gate-Source Voltage

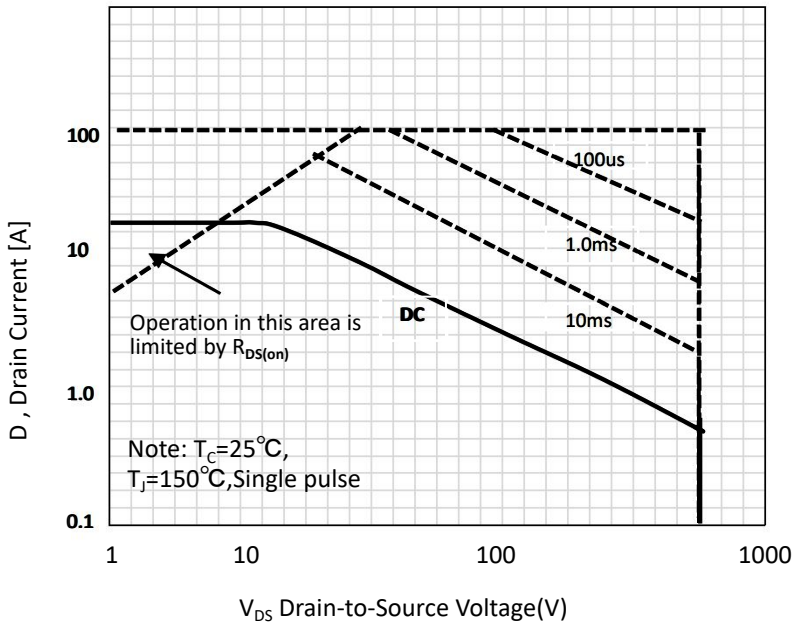


Figure 7. Maximum Safe Operating Area

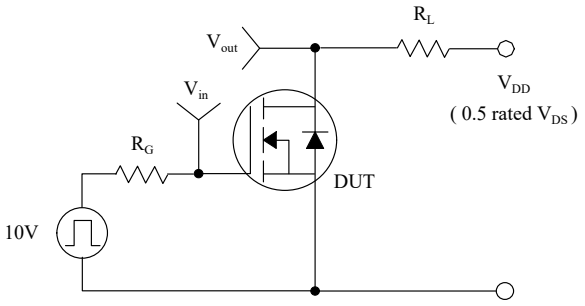


Figure 8 a. Switching Time Test Circuit

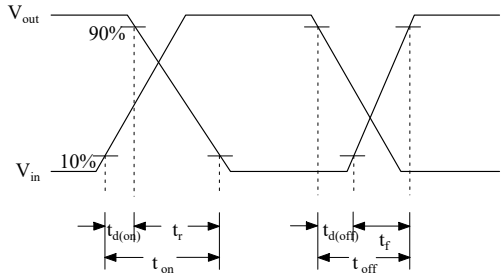


Figure 8 b. Switching Time Waveforms

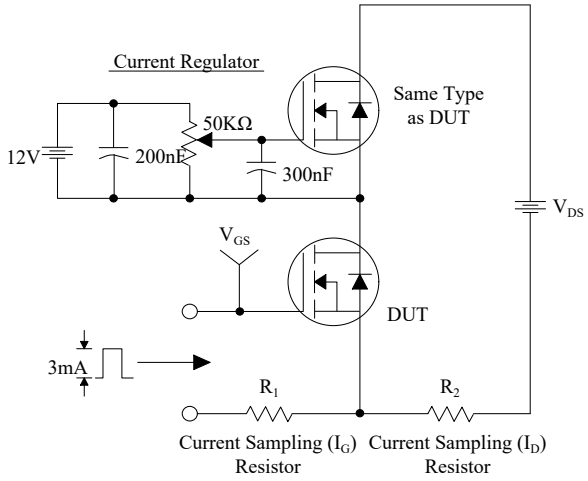


Figure 9 a. Gate Charge Test Circuit

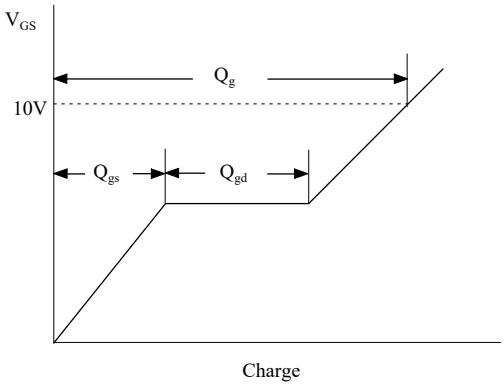


Figure 9 b. Basic Gate Charge Waveforms

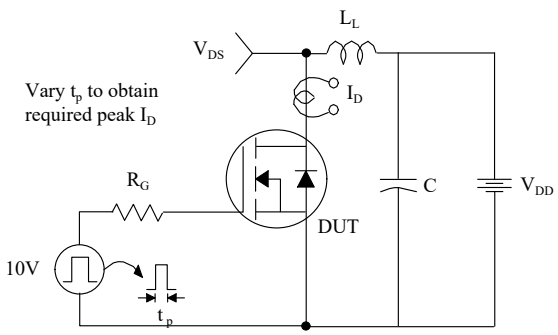


Figure 10 a. Unclamped Inductive Switching Test Circuit

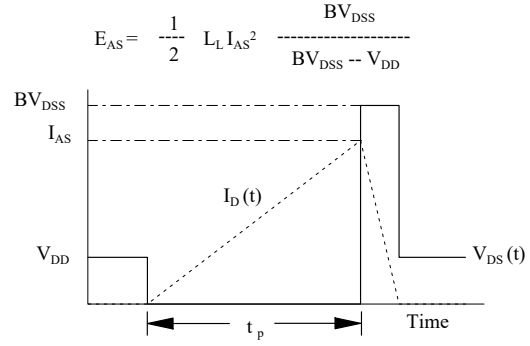


Figure 10 b.witching Test Waveforms